

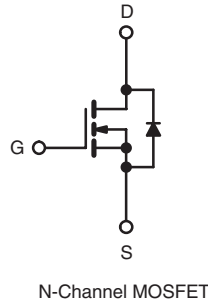


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Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	600
R _{DS(on)} (Ω)	V _{GS} = 10 V 4.4
Q _g (Max.) (nC)	18
Q _{gs} (nC)	3.0
Q _{gd} (nC)	8.9
Configuration	Single

TO-220 FULLPAK



FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. The isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

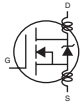

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIBC20GPbF SiHFIBC20G-E3
SnPb	IRFIBC20G SiHFIBC20G

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	600	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A	
		T _C = 100 °C		
Pulsed Drain Current ^a	I _{DM}	6.8		
Linear Derating Factor		0.24	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}	84	mJ	
Repetitive Avalanche Current ^a	I _{AR}	1.7	A	
Repetitive Avalanche Energy ^a	E _{AR}	3.0	mJ	
Maximum Power Dissipation	T _C = 25 °C	P _D	30	W
Peak Diode Recovery dV/dt ^c		dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d		
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 50 V, starting T_J = 25 °C, L = 53 mH, R_G = 25 Ω, I_{AS} = 1.7 A (see fig. 12).
- I_{SD} ≤ 2.2 A, dI/dt ≤ 40 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	4.1	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.88	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.0\text{ A}^b$	-	-	4.4	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 1.0\text{ A}^b$		1.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	350	-	pF
Output Capacitance	C_{oss}			-	48	-	
Reverse Transfer Capacitance	C_{riss}			-	8.6	-	
Drain to Sink Capacitance	C	$f = 1.0\text{ MHz}$		-	12	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 2.0\text{ A}, V_{DS} = 360\text{ V}$, see fig. 6 and 13 ^b	-	-	18	nC
Gate-Source Charge	Q_{GS}			-	-	3.0	
Gate-Drain Charge	Q_{GD}			-	-	8.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 2.0\text{ A}, R_G = 18\text{ }\Omega, R_D = 150\text{ }\Omega$, see fig. 10 ^b		-	10	-	ns
Rise Time	t_r			-	23	-	
Turn-Off Delay Time	$t_{d(off)}$			-	30	-	
Fall Time	t_f			-	25	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.7	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	6.8	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 1.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.0\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	290	580	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.65	1.3	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



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IRFIBC20G, SiHFIBC20G

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

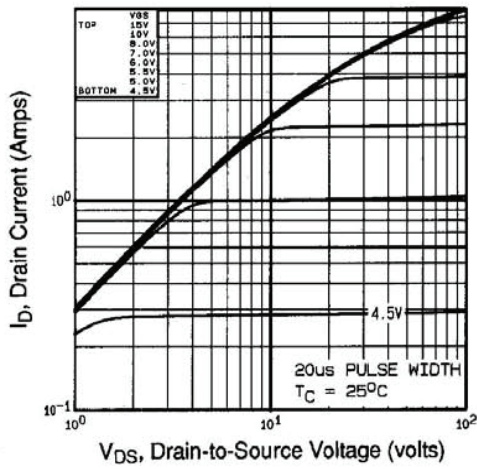


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

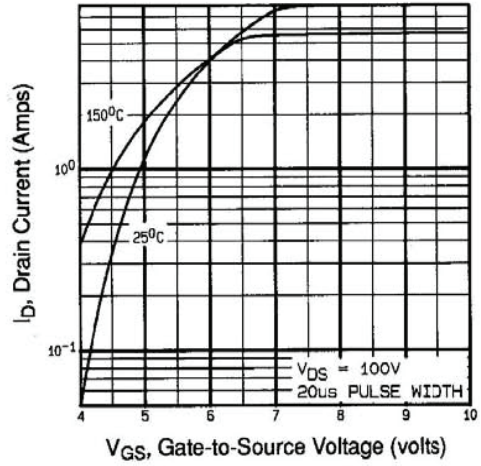


Fig. 3 - Typical Transfer Characteristics

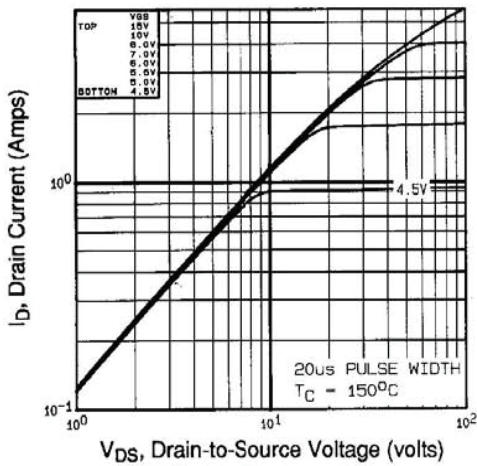


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

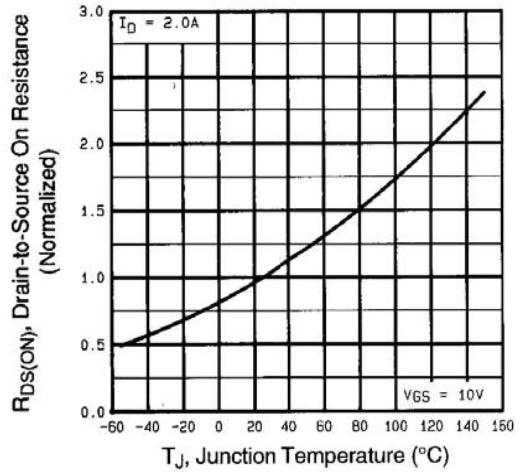


Fig. 4 - Normalized On-Resistance vs. Temperature

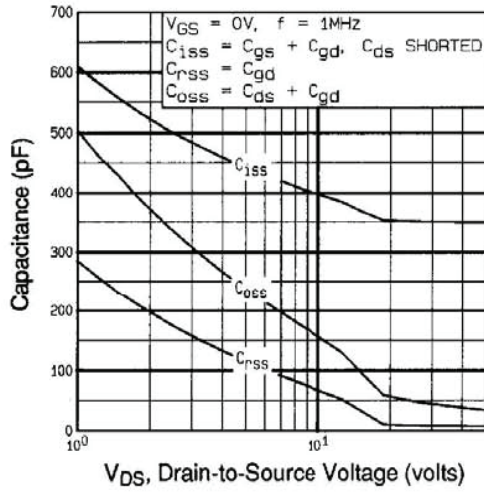


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

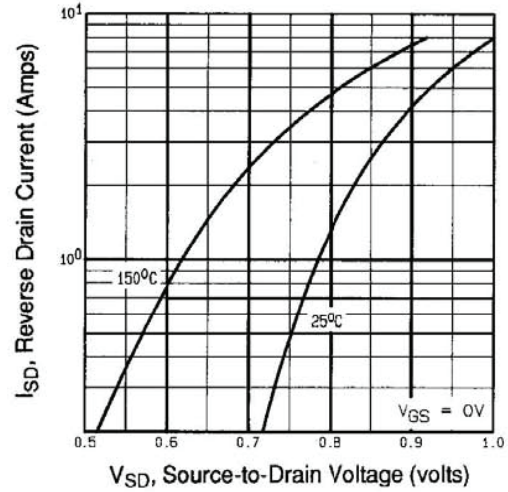


Fig. 7 - Typical Source-Drain Diode Forward Voltage

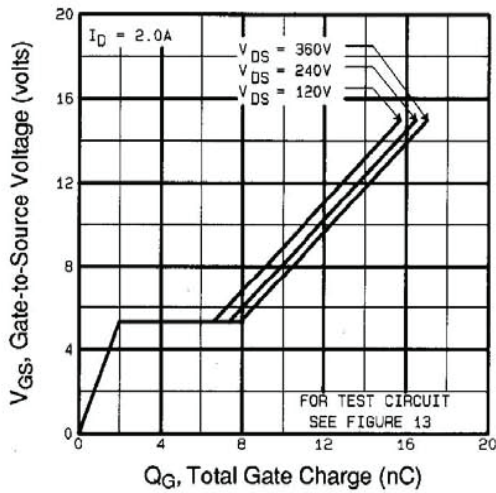


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

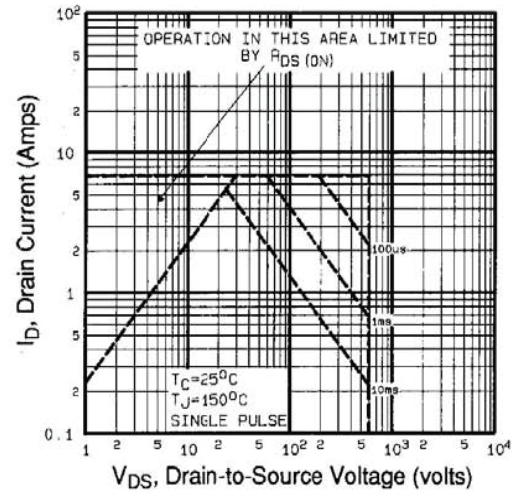


Fig. 8 - Maximum Safe Operating Area



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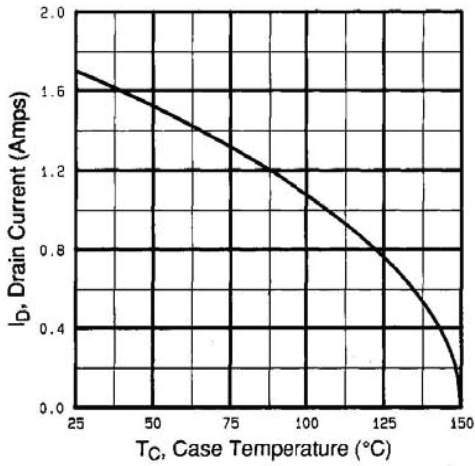


Fig. 9 - Maximum Drain Current vs. Case Temperature

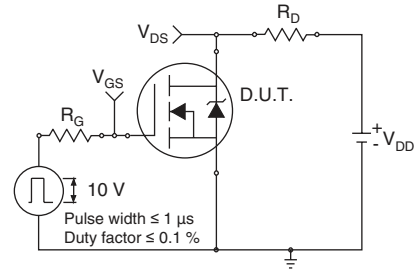


Fig. 10a - Switching Time Test Circuit

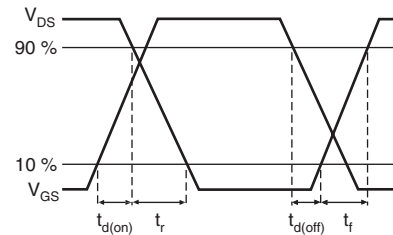


Fig. 10b - Switching Time Waveforms

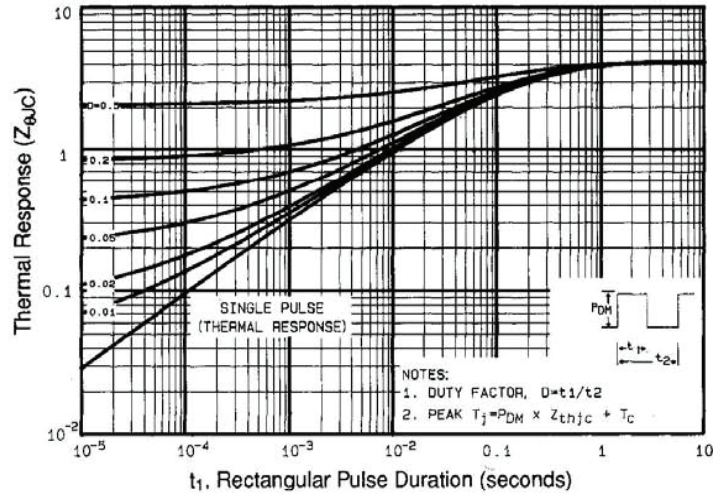


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

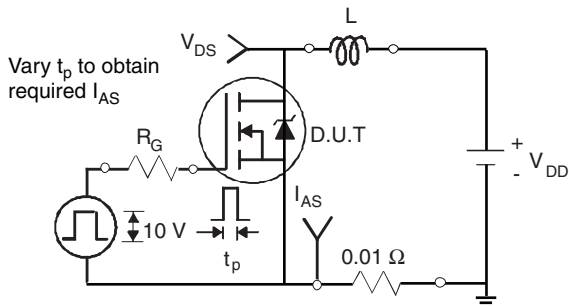


Fig. 12a - Unclamped Inductive Test Circuit

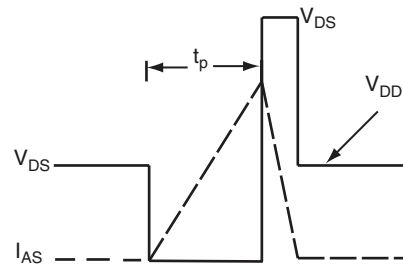


Fig. 12b - Unclamped Inductive Waveforms

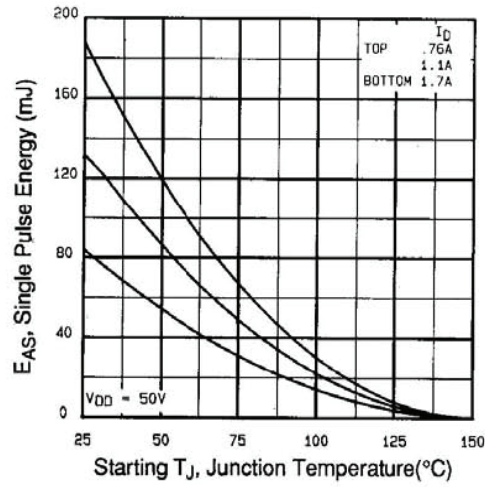


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

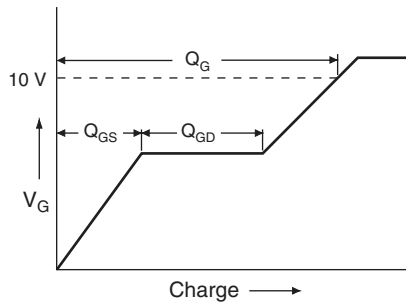


Fig. 13a - Basic Gate Charge Waveform

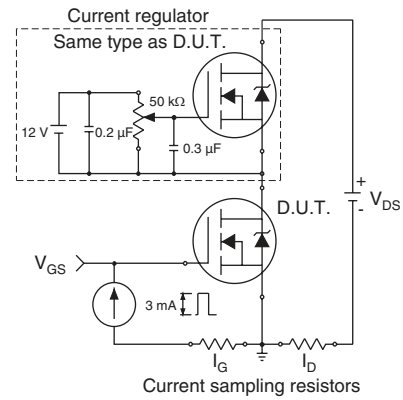
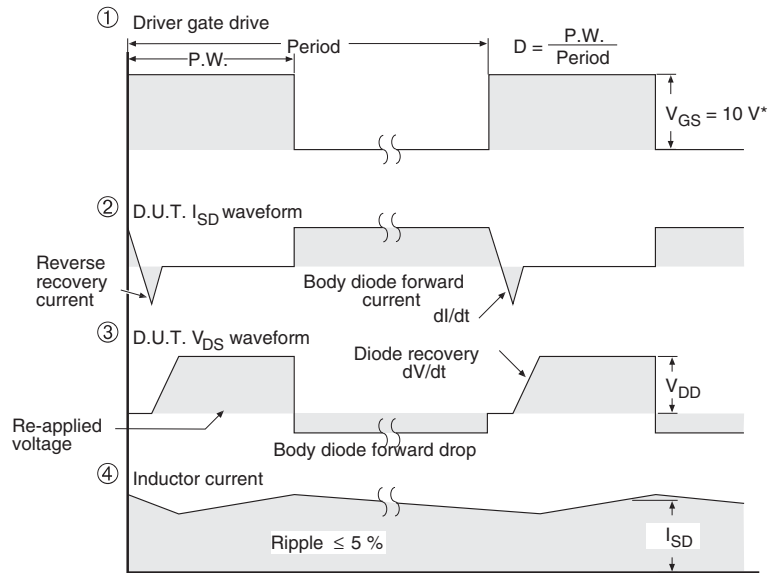
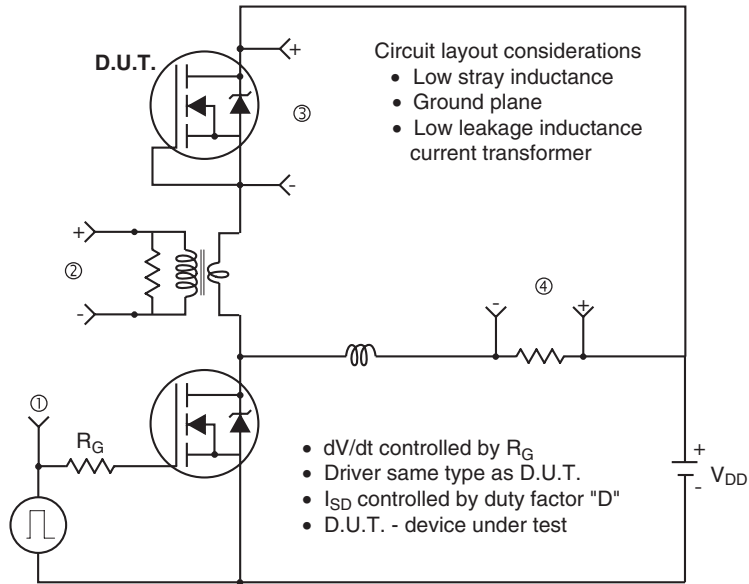


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel